JOURNAL OF TELECOMMUNICATIONS AND INFORMATION TECHNOLOGY

Preface

Despite the fact that a range of limitations are beginning to appear as CMOS technology is being raised to ever higher levels of perfection, it is anticipated that silicon will be the dominant material of the semiconductor industry for at least the first half of the 21st century. The forecast for microelectronics development published in 2006 by Semiconductor Industry Association (SIA) reaches ahead to the years 2014–2020. Moreover, a comparison with former SIA forecasts indicates that they become more aggressive (that is more optimistic) with time.

While the development of silicon microelectronics in the past could be attributed mostly to the reduction of the feature size (progress in lithography), today it relies more on new material solutions, such as SOI, SON, SiGe or SiC. The combination of this trend with continuous miniaturization provides the opportunity of improving IC functionality and speed of operation.

Telecommunications and information technology are arguably the most powerful drivers behind microelectronics product development nowadays. Plenty of new applications are being created for fast analog and rf circuits, as well as for information processing ones. It is clear that with the anticipated peak $f_{\max} = 425$ GHz and $f_T = 385$ GHz to be reached by rf SiGe-base bipolar transistors in 2011, according to the 2006 issue of ITRS, a lot of effort must be put into the development of appropriate material, processing, characterization and modeling. While progress in the bipolar technology is impressive, the increase of MOSFET speed is even more so. The same issue of ITRS predicts on-chip clock of 73 GHz for 2020, which will require MOSFET internal switching speed of 12 500 GHz.

High-speed isn't, however, everything. Portable wireless products push, for obvious reasons, for low-power solutions. This trend requires new architectural solutions (e.g., channel thinning), and in consequence, new material, such as SOI (or its possible successor SON), where current driveability is considerably higher than in conventional MOSFETs.

In this issue the Reader will find papers devoted to fabrication (ultra-thin gate dielectrics, DLC and BN layers), characterization (influence of strain on the optical properties of the Si-SiO_2 system, non-uniformity of MOSFET electrical parameters over the gate area,

quality of the dielectric-semiconductor interface) and modeling (strained-Si, SiC MOSFETs) of semiconductor devices. Statistical modeling of process (Monte Carlo) and IC reliability is also addressed, as well as optical interconnects in future ICs.

We hope the Readers will find this issue of the *Journal of Telecommunications and Information Technology* useful and interesting.

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